Title: **POWER MANAGEMENT MECHANISM FOR LOOP POWERED TIME OF FLIGHT AND LEVEL MEASUREMENT SYSTEMS**

RELATED APPLICATION

This application claims the benefit under 35 U.S.C. §119 of foreign patent application serial no. 2,406,298 filed on September 30, 2002 in Canada, which is incorporated herein by reference.

FIELD OF THE INVENTION

[0001] The present invention relates to time of flight ranging systems and level measurement systems, and more particularly to a power management mechanism and technique for loop powered level measurement systems.

BACKGROUND OF THE INVENTION

[0002] Loop powered level measurement systems operate on a 4-20mA current loop, hence the name loop powered. The circuitry for the level measurement system, i.e. the load, is typically designed to operate at less than 4 mA. The current loop provides a terminal voltage in the range 12-30V, but is nominally 24V.

[0003] To take a measurement, power is applied to the transducer and the reflected pulses are detected and the distance to the reflective surface is calculated or measured. If more than 4mA is needed to make a measurement, then energy taken from the current loop is stored until there is enough to make the measurement. In addition, to make rapid measurements, more current from the loop is also needed. As the current in the loop increases, the speed of measurement also increases. Since the power available from the current loop is less than the power required to continuously operate the level measurement device, the level measurement device is operated intermittently. In a typical level measurement system, measurements are taken once every second up to once every five seconds.

[0004] Accordingly, there remains a need for power management in the field of loop powered level measurement or time of flight ranging systems.

BRIEF SUMMARY OF THE INVENTION

[0005] The present invention provides a mechanism and method for power management in a level measurement or time of flight ranging system.

[0006] In a first aspect, the present invention provides a level measurement system, the level measurement system is powered by a two wire loop, the level measurement system comprises: (a) a transducer for emitting energy pulses and detecting reflected energy pulses; (b) a controller having a component for controlling the transducer, and a component for determining a level measurement based on the time of flight of the reflected energy pulse; (c) a power supply having an input port for receiving power from the loop, and a component for producing an output voltage; (d) a power management unit coupled to the loop, the power management unit having an output coupled to a storage capacitor for charging the storage capacitor, an input port for receiving excess power from the loop; (e) the transducer including an input for receiving energy from the storage capacitor under the control of the controller.

[0007] In another aspect, the present invention provides a level measurement system, the level measurement system is powered by a current loop, the level measurement system comprises: (a) a transducer for emitting energy pulses and detecting reflected energy pulses; (b) a controller with a component for controlling the transducer, and a component for determining a level measurement based on the time of flight of the reflected energy pulse; (c) a power supply having an input port coupled the current

loop for receiving current at a voltage level, and the power supply having a component for producing an output voltage for powering the controller; (d) a power management unit coupled to the current loop, the power management unit having an output coupled to a storage capacitor for charging the storage capacitor, an input port for receiving excess current from the current loop; (e) the transducer includes an input for receiving energy from the storage capacitor under the control of the controller.

[0008] Other aspects and features of the present invention will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Reference is next made to the accompanying drawings, which show, by way of example, embodiments of the present invention and in which:

[0010] Fig. 1 shows in diagrammatic form a loop powered level measurement system and power management mechanism according to the present invention.

[0011] Fig. 2 shows in block diagram form the loop powered level measurement system according to the present invention;

[0012] Fig. 3 shows in schematic form an implementation for the power management circuitry the level measurement system in Fig. 2.;

[0013] Fig. 4 shows in schematic form a circuit implementation for the waste power supply module; and

[0014] Fig. 5 shows in schematic form a circuit implementation for the shunt current regulator.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0015] Reference is first made to Fig. 1 which shows a loop powered level measurement system with power management according to the present invention. The loop powered level measurement system, indicated generally by reference 10, interfaces to a power/communication loop 20, for example a 4-20mA current loop. The loop powered level measurement system 10 is coupled to the current loop 20 at terminals A and B. A remote receiver, for example a plant control computer, indicated by reference 8 is coupled at the other end of the current loop 20. For a typical 4-20mA current loop configuration, the loop 20 provides a current in the range 4 to 20mA and a loop voltage in the range 18 to 30 Volts. The loop voltage is nominally at 24 Volts and represented as a voltage source with reference 22. The resistance of the loop is represented as a resistive element 24 and is typically in the range 0 to 550 Ohms. While the loop current is normally in the range 4 to

20mA, the current may range from 3.6 to 21.6mA to indicate alarm conditions.

[0016] Reference is next made to Fig. 2 which shows in more detail the level measurement system with power management 10 according to the invention. The level measurement system 10 comprises a transducer module 101, a controller 102, a power supply 104, a shunt current regulator 106, a loop current sensor and amplifier circuit 108, a power management module 110 and an energy storage capacitor 112. The level measurement system 10 may also include a communication module 114.

[0017] The power supply 104 comprises a switching power supply and is designed to consume less than the minimum loop current, nominally 4 mA.

[0018] The shunt current regulator 106 is operated under firmware control by the controller 102 to draw additional current to achieve the desired current in the current loop 20. One terminal of the shunt current regulator 106 is connected to terminal A of the current loop 20 and the input to the power supply 104. The other terminal of the shunt current regulator 106 is coupled to the power management module 110. The shunt current regulator 106 has a control terminal which is coupled to a control output port on the controller 102. The shunt current regulator 106 is also used by the power management module 110 to charge the storage capacitor 112 as described in more detail below. The loop current sensor and amplifier circuit 108 senses the current flowing in the loop 20 and provides feedback for the shunt current regulator 106 and the controller 102. The loop current sensor

and amplifier circuit 108 may be implemented with a current sensing resistor and an amplifier as shown in Fig. 4.

[0019] As shown in Fig. 2, the level measurement system 10 also includes a user interface module 116. The user interface module 116 comprises a display, for example, a LCD module, and a keypad or touch sensitive overlay on the LCD.

[0020] The transducer module 101 is coupled to a control port and input/output port on the controller 102. The transducer module 101 includes a transducer, a transmitter stage and a receiver stage (not shown). The transducer (not shown) may comprise radar-based technology, ultrasonic-based technology, TDR-based technology (time domain reflective), or other distance ranging technology. Under the control of a program stored in memory (e.g. firmware), the controller 102 generates a transmit pulse control signal for the transmit stage in the transducer module 101, and the transducer (not shown) emits a transmit burst of energy, for example, radar pulses directed at the surface of a material 50 (Fig. 1) contained in a storage vessel 60 (Fig. 1). The reflected or echo pulses, i.e. the propagated transmit pulses reflected by the surface 52 of the material 50 (Fig. 1), are coupled by the transducer, for example, a radar antenna or other distance ranging technology (not shown), in the transducer module 101 and converted into electrical signals by the receiver stage (not shown). The electrical signals are inputted by the controller 102 and sampled and digitized by an A/D converter (not shown) and a receive echo waveform or profile is generated. The controller 101 executes an algorithm which identifies and verifies the echo pulse and calculates the range, i.e. the distance to the reflective surface, from the time it takes for the reflected energy pulse to travel from

the reflective surface 52 (Fig. 1) to the transducer (not shown) in the transducer module 101. From this calculation, the distance to the surface of the material 50 and thereby the level of the material 50 in the vessel 60 is determined. The controller 101 may comprise a microprocessor or a microcontroller with on-chip resources, such as an A/D converter, ROM (EPROM), RAM. The microprocessor or microcontroller is suitably programmed to perform these operations as will be within the understanding of those skilled in the art.

[0021] Referring to Fig. 2, all power for the operation of the level measurement system 10 is derived from the current loop 20. The power supply module 104 comprises a switching power supply which takes its power input from the current loop 20 and generates the appropriate voltage levels, e.g. supply rails, for the circuitry, i.e. the controller 102, the display and user interface module 106 and the other electronic modules in the level measurement system 10. The transducer module 101 is powered from the waste power supply 110 as described in more detail below.

[0022] The controller module 102 also controls the transmission of data and control signals through the interface with the current loop 20. The controller 102 uses the shunt current regulator 106 to adjust or modulate the loop current in the range 4 to 20mA to transmit the calculated level of the material 50 to the remote receiver or plant computer 8 (Fig. 1) connected to the other end of the current loop 20 (Fig. 1). As shown in Fig. 2, the level measurement system 10 may include the communication module 114. The communication module 114 includes a digital communication modem, for example a HART modem, which provides another communication channel

between the controller 102 and the remote computer 8 (Fig. 1) over the wires of the current loop 20.

[0023] In operation, the user interface module 116 comprising the display module and the keypad, and the digital communication module 114 are run continuously. The display, user interface and communication operations may be thought of as primary functions which run continuously. The transducer module 101 is operated intermittently to transmit energy pulses and detect reflected energy pulses from the surface of the material 50 contained in the vessel 60.

[0024] The power available from the current loop 20 for the level measurement system 10 is given by:

(loop voltage – (loop current x loop resistance)) x loop current

In order to achieve the fastest operation rate, all available power from the current loop 20 is utilized by the level measurement system 10.

[0025] The power management module 110 functions to tap excess power, e.g. loop current > main power supply 104, from the current loop 20, as will be described in more detail below. As shown in Fig. 2, the power management module 110 is coupled to the storage capacitor 112 and the shunt current regulator 102.

[0026] The power management module 110 uses the shunt current regulator 102 to charge the storage capacitor 112. The power supply 104 is

designed to operate at less than the lower current loop limit, for example, 3 mA, which means that at least 1 mA of loop current is shunted by the shunt current regulator 106 and to the power management module 110 to charge the storage capacitor 112. As shown, the controller 102 has an input port coupled to the storage capacitor 112. The controller 102 senses the voltage on the storage capacitor 112. When the voltage level on the capacitor 112 is sufficient to power the transducer module 101, the controller 102 activates the transducer 101 to perform a level measurement for the vessel 60 (Fig. 1). The controller 102 then deactivates the transducer module 101 and the capacitor 112 is allowed to recharge using the power management module 110. The level measurement calculated by the controller 102 is transmitted to the remote computer 8 (Fig. 1) as a communication task for the primary functions. It is not necessary to turn off the controller 102 between measurements, and the controller 102 continues to execute the refresh operation and keypad scan functions for the user interface module 116, and the communication function.

[0027] Reference is next made to Fig. 3, which shows in schematic form a circuit implementation for the waste power supply module 110. As shown in Fig. 3, the waste power supply 110 comprises a regulator circuit 202 and a clamp circuit 204. In the waste power supply 110, terminal 206 (PRAW) is coupled to the shunt regulator 106 (Fig. 2) and the storage capacitor 112 (Fig. 2). Terminals 208 (COM) are connected to the common rail (COM) for the system 10. One terminal of the loop current sensor 108 (Fig. 2, Fig. 4). Terminal 210 (CLAMP*) is coupled to the controller 102 (Fig. 2), and driven by the controller 102 during start-up. Terminal 212 (PHV) is coupled to terminal A (Fig. 1).

[0028] In operation, the regulator circuit 202 tries to maintain PRAW, i.e. terminal 206, approximately 2 Volts below PHV, i.e. terminal 212. As the voltage on PRAW drops to 2 Volts less than the voltage on PHV, diodes D10 and D11 begin to turn off, which causes transistors Q9 and Q6 to turn. With the transistors Q6 and Q9 on, the impedance between PRAW and COM_CAP is reduced. This tends to increase the voltage difference between PRAW and PHV, thereby maintaining an approximate 2 Volt difference between PRAW and PHV.

[0029] In the operation of the clamp circuit 204, when the terminal 210, i.e. CLAMP*, is LOW, resistors R31 to R36 connected in series with diode D13 are coupled across terminal A and the common rail COM. This provides a load while the controller 102 is starting up or initializing. The terminal 210 or CLAMP* is maintained low during start up, and when CLAMP* is high the load from resistors R31-R36 is disconnected. This load on start up is provided to ensure a current draw greater than 22.6 mA from the current loop 20.

[0030] Reference is next made to Fig. 4 which shows a circuit implementation for the loop current sensor and amplifier circuit 108. The loop current sensor and amplifier circuit 108 comprises a resistor 220 and an operational amplifier circuit 222. The loop current sensor 108 has terminal 224 (NEG), terminal 226 (COM), and output terminal 228 (LOOP_SENSE). The NEG terminal 224 is coupled to terminal B (Fig. 2) and the current loop 20 (Fig. 1). The COM terminal 226 is connected to the common or return supply rail. The LOOP_SENSE terminal 228 provides the output for the loop current sensor 108 and is formed from the output of the operational amplifier

in the circuit 222. The LOOP_SENSE terminal is coupled to an input on the shunt current regulator 106 as shown in Fig. 5.

[0031] Reference is next made to Fig. 5, which shows a circuit implementation for the shunt current regulator 106. The shunt current regulator 106 as shown in Fig. 5 comprises a Pulse Width Modulator (PWM) circuit 230, an error amplifier circuit 232, a controlled current source 234, and a filter and voltage drop circuit 236.

[0032] The PWM filter circuit 230 has an input terminal (PWM) 240, and an output terminal (ANALOG_OUT) 242. The PWM terminal 240 is coupled to an output port on the controller 102 (Fig. 2) which is used to set the current level, i.e. between 4 to 20 mA. The ANALOG_OUT terminal 242 is coupled to the "Modulate" signal port on the HART modem 114 (Fig. 2). In operation, the PWM filter circuit 230 low pass filters the PWM signal on the input terminal 240 to produce a DC voltage, i.e. PWM output, which is proportional to the duty ratio or duty cycle of the PWM signal received from the controller 102 (Fig. 2).

[0033] The error amplifier circuit 232 has an input terminal (CURRENT_SENSE) 244, terminal (PHV) 246, terminal (PRAW) 248, and terminal (PHFV) 250. The CURRENT_SENSE input terminal 244 is coupled to the LOOP_SENSE output terminal 228 (Fig. 4) from the loop current sensor 108. The PHV terminal 246 is coupled to the terminal A (Fig. 2). The error amplifier circuit 232 amplifies the difference between the actual current, i.e. as indicated by the input CURRENT_SENSE 244, and the requested current, i.e. the PWM output from the PWM filter circuit 230 which is

generated from the input PWM 240. This difference is used in the feedback loop to control the loop current.

[0034] The controlled current source circuit 234 is coupled to the output of the error amplifier 232. The controlled current source 234 is connected to the PHV terminal 246. The controlled current source 234 also includes terminal (PRAW) 248. The PRAW terminal 248 connects to the corresponding PRAW terminal 206 in the waste power supply 110 (Fig. 3). As shown the controlled current source circuit 234 includes a number of JFET transistors 254, indicated individually as 254a, 254b, 254c, 254d, 254e which are coupled in parallel. The parallel arrangement of the JFET transistors 254 allows for higher saturation currents.

[0035] The filter and voltage drop circuit 236 is coupled to terminal PHV 246 and includes a BIAS terminal 250 and a terminal (PHVF) 252. As also shown, the filter and voltage drop circuit 236 includes an inductor (L11) 256, a diode circuit 258 comprising diodes 260a, 260b, 260c, 260d, and a capacitor (C65) 262. The arrangement of the inductor 256 and the capacitor 262 filters noise arising from the power supply 104 from feeding back in the current loop. The diode circuit 258 is provided for clamping the inductor 256 for intrinsically safe, i.e. I.S., applications as required. The remainder of the circuit 236 as shown in Fig. 5 provides a voltage drop of approximately 0.7 Volts between the PHV terminal 246 and the PHVF terminal 252 as required for operation of the HART modem 114 (Fig. 2).

[0036] In operation, the less current the main power supply 104 draws from the loop 20, the more loop current flows to the shunt current regulator

106 and to the power management module 110 for faster charging of the storage capacitor 112. The faster the charging of the capacitor 112, the shorter the level measurement cycle. To improve charging efficiency, the power supply 104 is implemented as a switching power supply in the level measurement system 10. This means that as the loop voltage increases, the loop current drawn by the power supply 104 decreases resulting in an increase in the loop current to the shunt current regulator 106 and the power management module 110 for faster charging of the storage capacitor 112.

[0037] To further improve the charging efficiency of the storage capacitor 112, the microprocessor or microcontroller for the controller 102 may be operated at a slower clock speed, e.g. under control of the firmware and the instruction set specific to the microprocessor device. The microprocessor requires less current when operating at a slower clock speed. The primary functions, such as display, user interface and communications, can be performed at the slower clock speeds.

[0038] The present invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. Certain adaptations and modifications of the invention will be obvious to those skilled in the art. Therefore, the presently discussed embodiments are considered to be illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.